Dissertation / Project / Project Work Title:

Virtual prototyping and Emulation of conceptual IP

**Course No.** **ESZG628T**

**Course Title: Dissertation / Project / Project Work**

**Dissertation / Project /Project Work Done by:**

**Student Name: Senthil Kumar M**

**BITS ID: 2022HT01062**

**Degree Program: M.Tech in Embedded Systems**

**Research Area: Hardware and Software Co-Design**

**Dissertation / Project Work carried out at:**

**Analog Devices India Pvt Ltd, Banglore**



**BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI**

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**January 2024**

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# Broad Area of Work

This research project explores the implementation of the Fast Fourier Transform (FFT) algorithm on both the SystemC modeling platform and Field-Programmable Gate Arrays (FPGAs). The study delves into key aspects of the design process, comparing and contrasting the characteristics of SystemC, a high-level system modeling language, with the intricacies of FPGA hardware implementation.

The abstraction level of SystemC provides a conducive environment for rapid prototyping and iterative development. It allows for the high-level modeling of complex systems and algorithms, fostering flexibility and ease of design modifications. In contrast, FPGA implementation demands a low-level hardware description using Hardware Description Languages (HDLs), necessitating a more structured and rigorous development process.

Simulation and debugging play crucial roles in the design cycle. SystemC facilitates efficient simulation and debugging at a high level, offering user-friendly tools for analysis. On the other hand, FPGA debugging involves more intricate processes, including simulation before synthesis and the utilization of specialized hardware debugging tools.

Performance analysis is approached differently in each domain. SystemC allows for the estimation of timing and throughput at a system level, abstracting away detailed hardware characteristics. In FPGA design, precise performance metrics, including timing, throughput, and resource utilization, are critical considerations, with tools providing detailed reports on hardware resources.

The implementation of parallelism and pipelining is a notable distinction. While SystemC allows for the modeling of these concepts, FPGA inherently supports parallelism, and explicit implementation of pipelining is crucial for optimizing design efficiency.

Timing constraints and real-time analysis are fundamental aspects of both SystemC and FPGA design, but their treatment differs. SystemC abstracts timing constraints during simulation, while FPGA tools rigorously analyze and report timing violations, necessitating adjustments for compliance. Real-time requirements are a focal point for FPGA designs, requiring adherence to stringent timing constraints.

Power analysis, another critical consideration, is approached differently in each context. SystemC provides high-level estimates based on simulation activities, while FPGA tools offer detailed insights into power consumption, including dynamic and static power.

# Background

Digital signal processing plays a crucial role in various applications, including communication systems, audio processing, and image processing. The FFT algorithm is fundamental for efficiently computing the discrete Fourier transform, and its implementation can benefit from both high-level system modeling (SystemC) and dedicated hardware (FPGA). Understanding the trade-offs and characteristics of each approach is essential for optimizing performance in signal processing applications.

# Objectives

The objectives of my project are as follows:

* + - To implement the FFT algorithm using SystemC for high-level system modeling.
    - To implement the FFT algorithm on FPGA, emphasizing low-level hardware description and optimization.
    - To compare and contrast the characteristics, advantages, and limitations of the SystemC and FPGA implementations.
    - To assess factors such as abstraction level, simulation capabilities, performance analysis, and real-time constraints in both approaches.

# Scope of Work

The scope includes developing detailed SystemC models for the FFT algorithm and translating these models into FPGA hardware using Hardware Description Languages (HDLs). The study encompasses simulation, debugging, and performance analysis in both environments. The research also explores the impact of parallelism, pipelining, timing constraints, and real-time requirements. Power consumption analysis is conducted for both SystemC simulation and FPGA hardware implementation

# Plan of Work

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| **Phases** | **Start Date-End Date** | **Work to be done** |
| Dissertation Outline | 13 Jan 2019 – 21 Jan 2019 | Literature Review and prepare Dissertation Outline |
| Design & Development | 22 Jan 2019 – 15 Feb 2019 | Design & Development Activity |
| Testing | 16 Feb 2019 – 13 Mar 2019 | Software Testing, User Evaluation & Conclusion |
| Dissertation Review | 14 Mar 2019-25 Mar 2019 | Submit Dissertation to Supervisor & Additional Examiner for review and feedback |
| Submission | 26 Mar 2019-30 Mar 2019 | Final Review and submission of Dissertation |

# Literature References

1. *Oppenheim, A. V., & Schafer, R. W. (2010). Discrete-Time Signal Processing. Pearson*
2. *Introduction to Reconfigurable computing: Architectures, Algorithms and Applications. Christophe Bobda, Springer, 2007.*
3. *Patrick R. Schaumont, A Practical Introduction to Hardware/Software Codesign, Springer, 2nd ed. 2013*

# Particulars of the Supervisor and Examiner

|  |  |  |
| --- | --- | --- |
|  | **Supervisor** | **Additional Examiner** |
| Name | Rajiv Nadig | Tony O Brien |
| Qualification | M Tech in VLSI Design Tool and Technology | Bachelor of Engineering in Electronic Engineering |
| Designation | Director, Digital Signal Engineering | Staff Engineer, Product Applications |
| Employing Organization and Location | Analog Devices Inc, Wilmington, USA | Analog Devices Inc, Cock, Ireland |
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# Remarks of the Supervisor

The study and project seem to very promising. The student had covered all the relevant literature review. The project is holding the current domain of research and justified the level of dissertation for master studies. The outcome covered by the project seems very interesting and include all the state of arts in today’s era of information science. The project also includes the user study on the working prototype. This activity completely validates the research project. This project also contains the prospect of publication in future. After the initial meeting with the student, I got an impression that she is hard working student and have the skills to implement the experiment in standard research paradigm. I approved the following project as the supervisor.

**Information about the Supervisor:**

Mr. Rajiv Nadig holds a postgraduate degree in VLSI design tools and technology from IIT Delhi and is a seasoned expert in the field of ASIC design. With over 23 years of experience, he has demonstrated his proficiency in VLSI design, specializing in various products, particularly in Analog design

**BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI**

**WORK INTEGRATED LEARNING PROGRAMMES (WILP) DIVISION**

**SECOND SEMESTER OF ACADEMIC YEAR 2021-2022**

**ESZG628T : M.Tech in Embedded Systems OUTLINE**

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| --- | --- |
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| **STUDENT’S EMPLOYING ORGANIZATION & LOCATION** | Analog Devices, India Pvt Ltd, Banglore |
| **SUPERVISOR’S NAME** | Rajiv Nadig |
| **SUPERVISOR’S EMPLOYING ORGANIZATION & LOCATION** | Analog Devices Inc, Wilmington, USA |
| **SUPERVISOR’S EMAIL ADDRESS** | rajiv.nadig@analog.com |
| **ADDITIONAL EXAMINAER’S NAME** | Tony O Brien |
| **ADDITIONAL EXAMINER’S EMPLOYING ORGANIZATION & LOCATION** | Analog Devices Inc, Cock, Ireland |
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| **DISSERTATION / PROJECT / PROJECT WORK TITLE** | Virtual prototyping and Emulation of conceptual IP |

Please prepare the outline as a separate document with the following sections along with the above identification information.

1. Cover Page with Student ID No., Name, Course Number, Course Title and Dissertation / Project / Project Work Title, Broad Academic Area of Work.

2. Background (Relevance of the Project to the current work environment in the employing organization)

3. Objectives

4. Scope of Work (To be done by the student independently)

5. Plan of Work (Work to be done during the semester)

6. Literature References

7. Particulars of the Supervisor and Additional Examiner

8. Remarks of the Supervisor

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| **Signature of Student** | **Signature of Supervisor** | **Signature of Additional Examiner** |
| **Name: M Senthil Kumar** | **Name: Rajiv Nadig** | **Name: Tony O Brien** |